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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/701,534	11/06/2003	James William Kretchmer	134765	8161

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GENERAL ELECTRIC COMPANY (PCPI)
C/O FLETCHER YODER
P. O. BOX 692289
HOUSTON, TX 77269-2289

EXAMINER	
LEE, HSIEN MING	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 03/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/701,534	KRETCHMER ET AL.
	Examiner	Art Unit
	Hsien-ming Lee	2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-27 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-27 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 1/6/03 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

HSIEN-MING LEE
PRIMARY EXAMINER

3/16/2005

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 110603.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 4-7, 10-13, 15-17, 20, 22, 25 and 27 are rejected under 35 U.S.C. 102(e) as being anticipated by Mouli et al. (US 2004/0089914).

In re claim 1, Mouli et al. teach a method for optical and electrical isolation between adjacent integrated devices (i.e. pixel cells, paragraph [0004]), the method comprising:

- forming at least one trench 328 through an exposed surface of a semiconductor wafer 320 by removing a portion of the semiconductor wafer material (Fig.2);
- forming an electrically insulating layer 327 (i.e. silicon oxide) on the sidewalls and the bottom of the at least one trench 328 (Fig.3);
- filling the at least one trench 328 by conformally depositing an optically isolating material 329 (Fig.4), wherein the optically isolating material 329 comprises a doped polysilicon (paragraph [0045]),wherein Mouli et al. disclose the isolation structure is to provide both electrical and optical isolation between pixels (paragraph [0004]); and
- planarizing the semiconductor wafer surface by removing the portion of the optically isolating material 327 above the exposed surface of the semiconductor wafer (Fig.4).

In re claims 4-5, Mouli et al. teach that the step of forming the electrically insulating layer 327 comprises growing silicon oxide (paragraph [0044]) on the sidewalls and the bottom of the at least one trench 328.

In re claim 6, Mouli et al. teach that the step of forming the electrically insulating layer 327 comprises depositing NO, ON or ONO (paragraph [0044]) on the sidewalls and the bottom of the at least one trench 328, wherein NO is known as silicon nitride/silicon oxide, ON is known as silicon oxide/silicon nitride and ONO is known as silicon oxide/silicon nitride/silicon nitride (paragraph [0035]).

In re claims 7, 10, Mouli et al. inherently teach that the optically isolating material 329 comprises an opaque material since the optically isolating material 329 comprises a doped polysilicon (paragraph [0045]) and is deposited conformally.

In re claim 11, Mouli et al. teach that the electrically insulating layer 327 comprises silicon oxide (paragraph [0044]) and the optically isolating material 329 comprises a polysilicon (paragraphs [0045] and [0010]).

In re claim 12, Mouli et al. teach that the at least trench 328 is located between a plurality of adjacent device sites (i.e. adjacent pixel cells) (last two lines in paragraph [0004]).

In re claim 13, Mouli et al. teach that the step of forming the at least trench 328 comprises selectively etching the semiconductor wafer 320 with reactive ion etching (RIE) process (paragraph [0043]).

In re claims 15-16, Mouli et al. inherently teach planarizing the semiconductor wafer by subjecting the portion of the optically isolating material 329 above the exposed surface of the semiconductor wafer to an etching process, i.e. planarizing the optically isolating material 329 to

a level is that coplanar to the exposed surface of the wafer 320 (Fig.4), wherein the planarization can be performed by CMP process (paragraph [0049]).

In re claim 17, Mouli et al. teach a microelectronic device comprising:

- at least two integrated devices (i.e. pixel cells), wherein the at least two integrated devices are located in a substrate 320; and
- at least one trench 328in the substrate 320, wherein the at least one trench 328 physically separates the at least two integrated devices, and the inside of the at least one trench 328 is coated with an electrically insulating material 327 and filled with an optically isolating material 329 that is conformally deposited (Fig.4).

In re claim 20, Mouli et al. teach that the electrically insulating layer 327 is a thermally grown silicon oxide (paragraph [0044]).

In re claim 22, Mouli et al. teach that the electrically insulating layer 327 comprises silicon nitride because Mouli et al. disclose that the electrically insulating layer 327 comprises NO, ON or ONO (paragraph [0044]), wherein NO is known as silicon nitride/silicon oxide, ON is known as silicon oxide/silicon nitride and ONO is known as silicon oxide/silicon nitride/silicon nitride.

In re claim 25, Mouli et al. also teach that the at least two integrated devices comprises photodiodes because Mouli et al disclose that the two integrated devices comprises pixel cells, which include photodiodes (last two lines in paragraph [0004] and paragraph [0003]).

In re claim 27, Mouli et al. also teach that the at least two integrated devices comprises an array of serially connected diodes working as a gate to metal-oxide-semiconductor filed effect transistor because Mouli et al. disclose the array of serially connected diodes working as a gate to a CMOS (paragraph [0043]).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2, 3, 18, 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mouli (US '914) in view of Kwak et al. (US 2002/0074556).

Mouli et al. do not teach that the substrate is either silicon carbide (claims 2 and 18) or gallium nitride (claims 3 and 19).

Kwak et al., in an analogous art of forming a diode, teach using either silicon carbide or gallium nitride as the substrate (paragraph 0008]).

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time of the invention was made, to use either silicon carbide or gallium nitride, as taught by Kwak et al., as the substrate of Mouli et al. since by this manner it would satisfy the voltage requirement of the device.

5. Claims 8-9, 14, 21, 23, 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mouli (US '914) in view of Lee (US 5,498,566).

In re claims 9, 21 and 23, Mouli et al. teach filling the trench 328 with the polysilicon 329 (paragraph [0045]) to form the trench isolation but do not teach that the polysilicon is a low pressure chemical vapor deposition (LPCVD) polysilicon.

Lee, however, in an analogous art of forming the trench isolation, teaches forming a electrically insulating 53 (oxide) in the trench 51a and 51b followed by filling the trench 51a and 51b with polysilicon 61 via LPCVD (Fig.2 and col. 6, lines 20-21,col. 7, lines 60-62).

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time of the invention was made, to use LPCVD process, as taught by Lee, for depositing the polysilicon of Mouli et al. in the trench, since by this manner it would satisfactory filling the trench for isolation purpose.

In re claims 8 and 24, these claims are prima facie obvious without showing that the claimed ranges achieve unexpected results relative to the prior art range. In re Woodruff, 16 USPQ2d 1935, 1937 (Fed. Cir. 1990). See also In re Huang, 40 USPQ2d 1685, 1688(Fed. Cir. 1996)(claimed ranges of a result effective variable, which do not overlap the prior art ranges, are unpatentable unless they produce a new and unexpected result which is different in kind and not merely in degree from the results of the prior art). See also In re Boesch, 205 USPQ 215 (CCPA) (discovery of optimum value of result effective variable in known process is ordinarily within skill of art) and In re Aller, 105 USPQ 233 (CCPA 1955) (selection of optimum ranges within prior art general conditions is obvious).

In re claim 14, Mouli et al do not teach oxidizing the portion of the optically isolating material above the exposed surface of the semiconductor wafer; and removing the oxidized portion of the optically isolating material.

Lee, however, teaches oxidizing the portion of the optically isolating material 61 above the exposed surface of the semiconductor wafer to form a thermal oxide 63 (Fig.2 and col. 8, lines 9-11).

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time of the invention was made, to further oxidizing the portion of the optically isolating material 329 above the exposed surface of the semiconductor wafer 320 in Mouli et al. to form the thermal oxide, as taught by Lee, and then proceed an additional step of removing the oxidized portion of the optically isolating material , since by this manner it would provide a planar surface for the subsequent processing steps.

6. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mouli et al. (US '914) in view of Meksavan at al. (US 6,547,146).

Mouli et al. teach that the microelectronic device comprises a photodiode (paragraph [0047]) but do not expressly disclose that the microelectronic device comprises photoemitters.

Meksavan et al., however, teach that the photoemitter is an art-recognized equivalence to the photodiode (col. 3, lines 42-43).

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time of the invention was made, to apply the teachings of Mouli et al. in the application of wherein the microelectronic device comprises the photoemitter, in light of Meksavan et al, for a reasonable expectation of success since photoemitter is an art-recognized equivalence to the photodiode.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hsien-ming Lee whose telephone number is 571-272-1863. The examiner can normally be reached on Tuesday-Thursday (8:00 ~ 6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hsien-ming Lee
Primary Examiner
Art Unit 2823

March 16, 2005

HSIEN-MING LEE
PRIMARY EXAMINER

3/10/2005